VLSI CAD ENGINEERING

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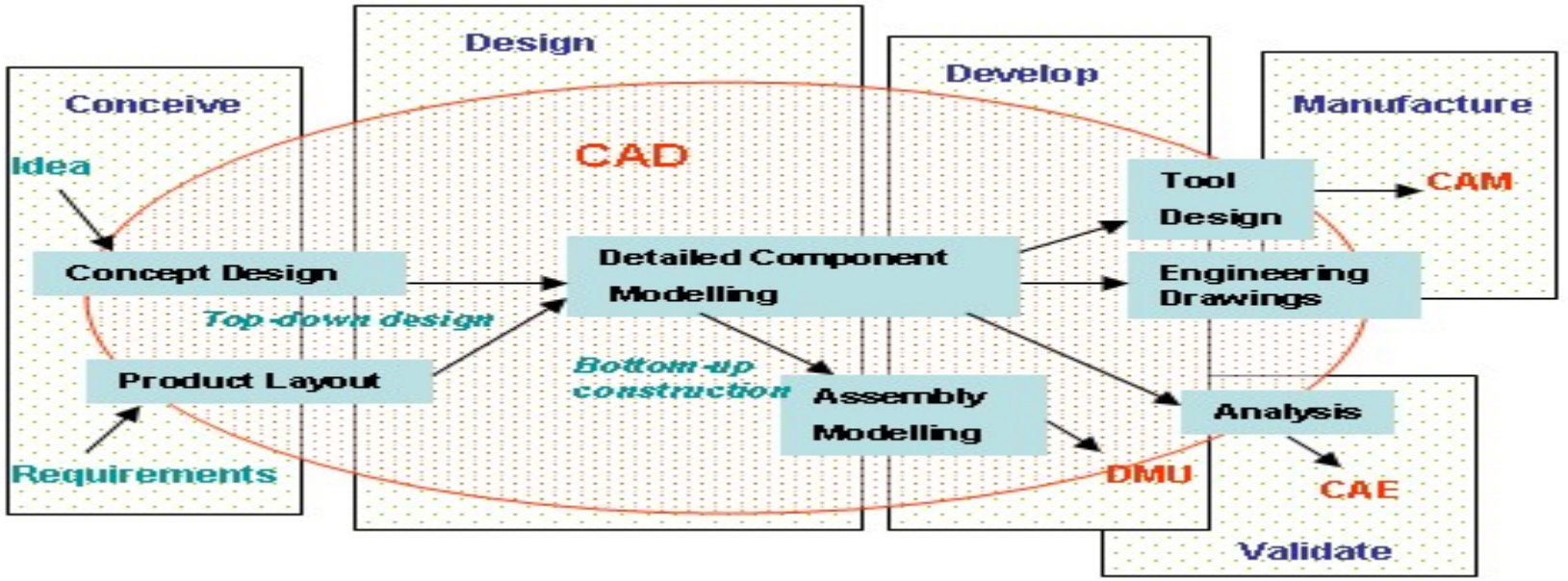
Agenda

- CAD (Computer-Aided Design)
  - General CAD
    - CAD innovation over the years (Short Video)
  - VLSI CAD (EDA)
    - EDA: Where Electronic Begins (Short Video)
    - Zoom Into a Microchip (Short Video)
- Introduction to Electronic Design Automation
  - Overview of VLSI Design Cycle
  - VLSI Manufacturing
    - Intel: The Making of a Chip with 22nm/3D (Short Video)
  - EDA Challenges and Future Trend
- VLSI CAD Engineering
  - EDA Vendors and Tools Development
  - Foundry PDK and IP Reuse
  - CAD Design Enablement
  - CAD as Career
- Q&A

CAD (Computer-Aided Design)

General CAD

- **Computer-aided design** (**CAD**) is the use of computer systems (or workstations) to aid in the creation, modification, analysis, or optimization of a design



CAD innovation over the years (Short Video)

- https://www.youtube.com/watch?v=ZgQD95NhbXk

CAD Tools

- **Commercial**
  - Autodesk AutoCAD
  - CAD International RealCAD
  - Autodesk Inventor
  - Bricsys BricsCAD
  - Dassault CATIA
  - Dassault SolidWorks
  - Kubotek KeyCreator
  - Siemens NX
  - Siemens Solid Edge
  - PTC PTC Creo (formerly known as Pro/ENGINEER)
  - Trimble SketchUp
  - AgiliCity Modelur
  - TurboCAD
  - IronCAD
  - MEDUSA
  - ProgeCAD
  - SpaceClaim
  - PunchCAD
  - Rhinoceros 3D
  - VariCAD
  - VectorWorks
  - Cobalt
  - Gravotech Type3
  - RoutCad RoutCad
  - SketchUp

- **Freeware and open source**
  - 123D
  - LibreCAD
  - FreeCAD
  - BRL-CAD
  - OpenSCAD
  - NanoCAD
  - QCad
- **CAD Kernels**
  - Parasolid by Siemens
  - ACIS by Spatial
  - ShapeManager by Autodesk
  - Open CASCADE
  - C3D by C3D Labs

VLSI CAD (EDA)

- Very-large-scale integration (**VLSI**) is the process of creating an integrated circuit (IC) by combining hundreds of thousands of transistors into a single chip.
- The design of **VLSI** circuits is a major challenge. Consequently, it is impossible to solely rely on manual design approaches. **Computer Aided Design** (**CAD**) is widely used, which is also referred as electronic design automation (**EDA**).

EDA: Where Electronic Begins (Short Video)

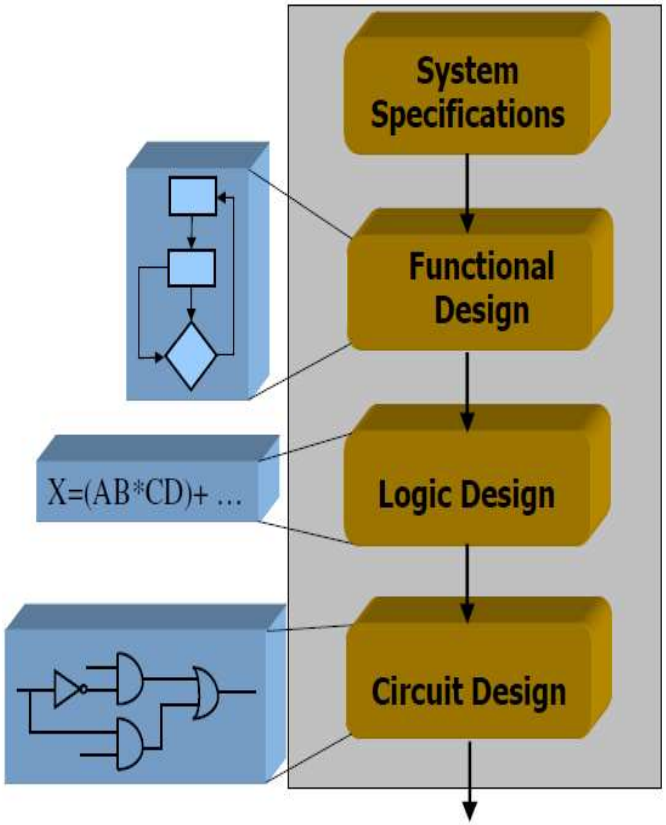
- https://www.youtube.com/watch?v=8uj81PWHlmk

Zoom Into a Microchip (Short Video)

- https://www.youtube.com/watch?v=Fxv3JoS1uY8

Introduction to Electronic Design Automation

Overview of VLSI Design Cycle



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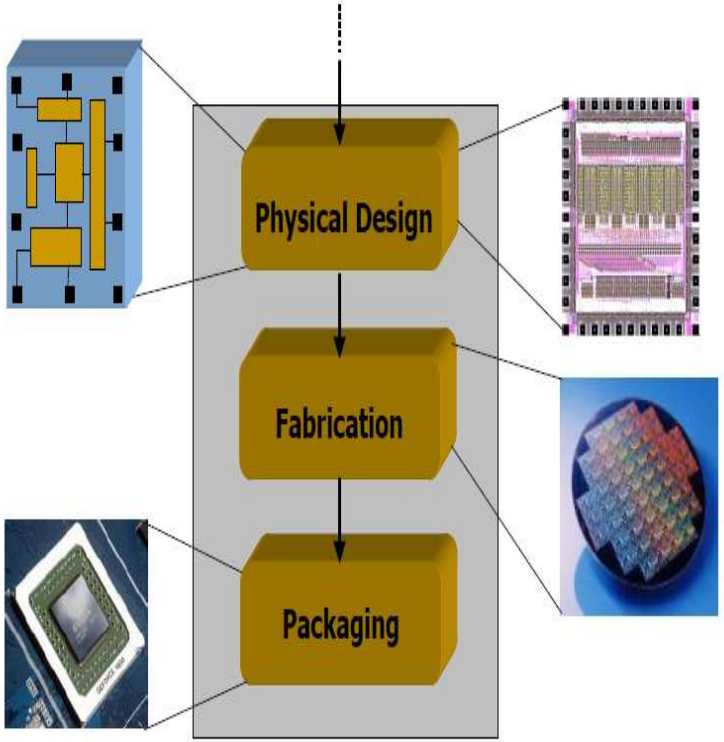
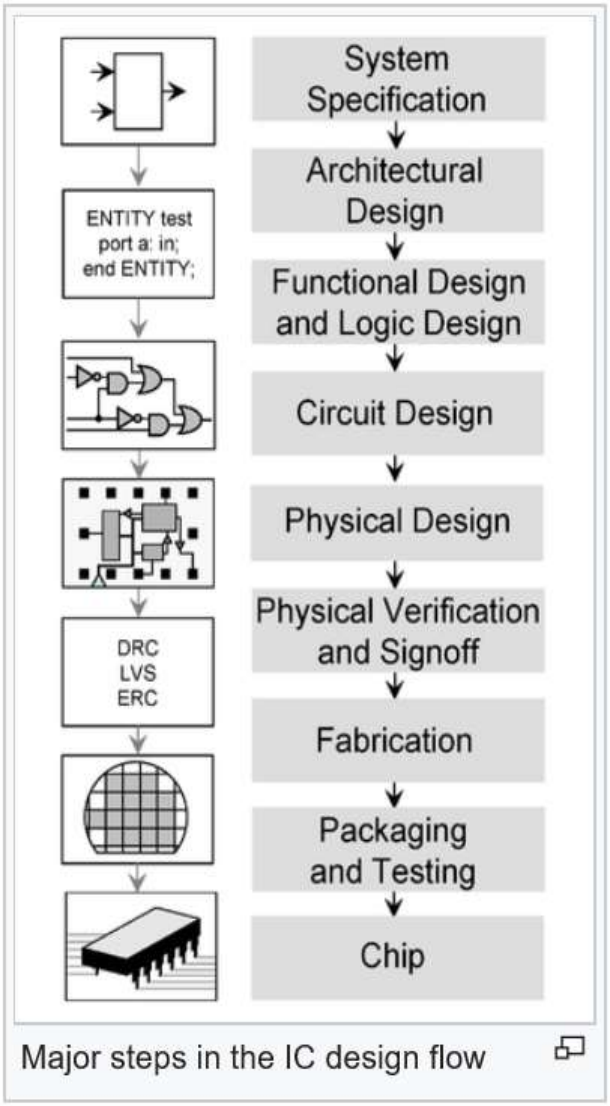


7 Major Steps in IC Design Flow

1. System specification
2. Functional design
3. Logic synthesis
4. Circuit design
5. Physical design and verification
6. Fabrication
7. Packaging

- Other tasks involved: testing, simulation, etc.
- Design metrics: area, speed, power dissipation, noise, design time, testability, etc.
- Design revolution: interconnect (not gate) delay dominates circuit performance in deep submicron era.
  - Interconnects are determined in physical design.
  - Shall consider interconnections in early design stages.



Major steps in the IC design flow

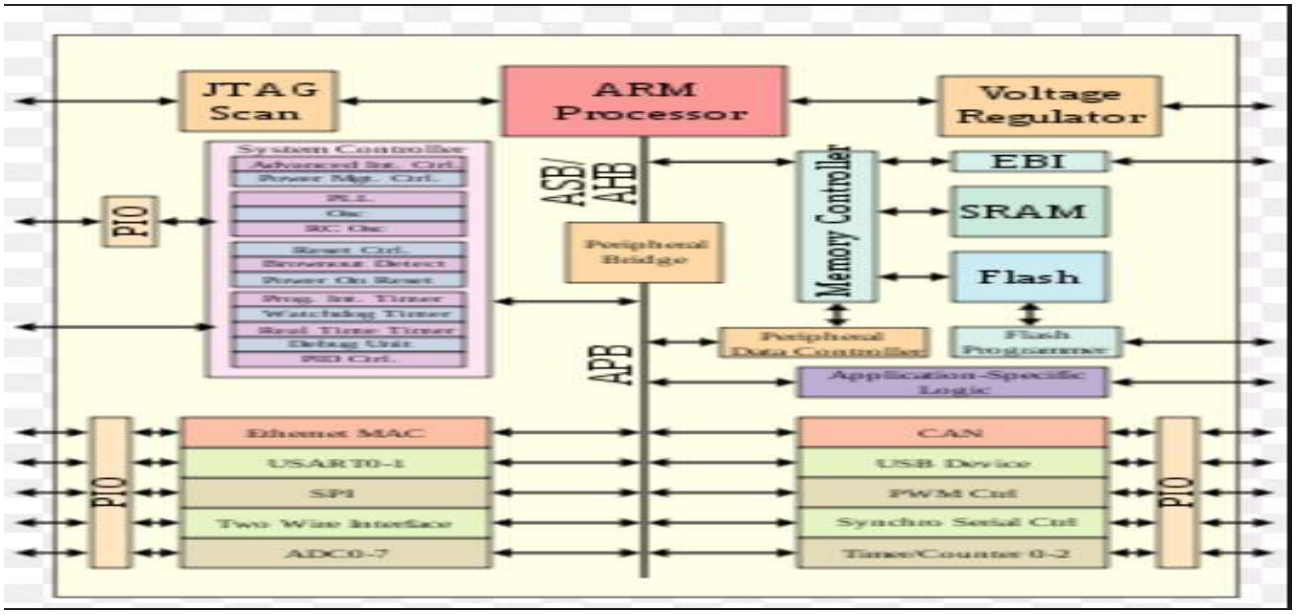
Step 1: System Specification

This is the crucial step as it will affect the future of the product. Here, vendors may want to get feedback from potential customers on what they are looking for

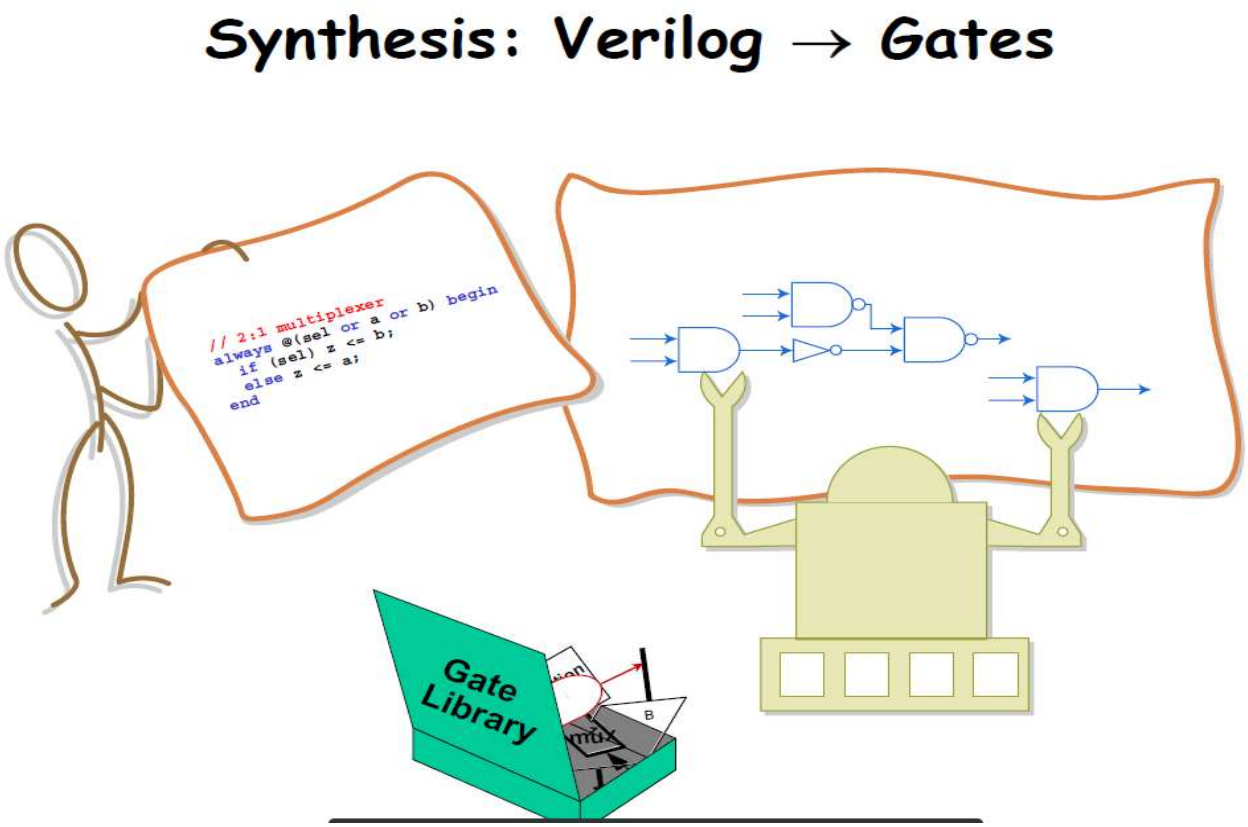
- **Instruction set**
- **Interface (I/O pins)**
- **Organization of the system**
- **Functionality of each unit in the system, and how to communicate it to other units.**

Step 2: Architectural Design

This is where the main work starts. With the help of the specification sheet the target IC's architecture is decided and a layout for same is created by design engineers using EDA tools.

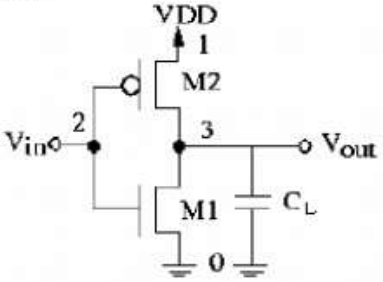


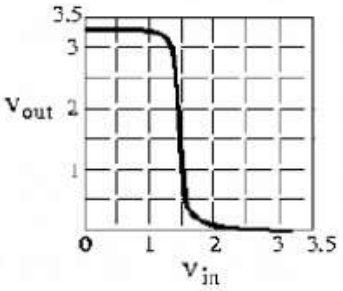
Step 3: Functional and Logic Design

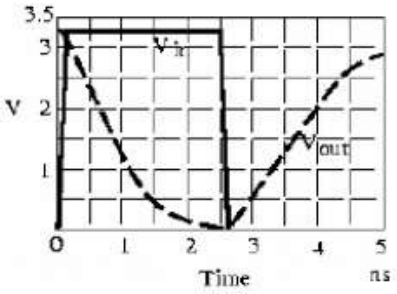


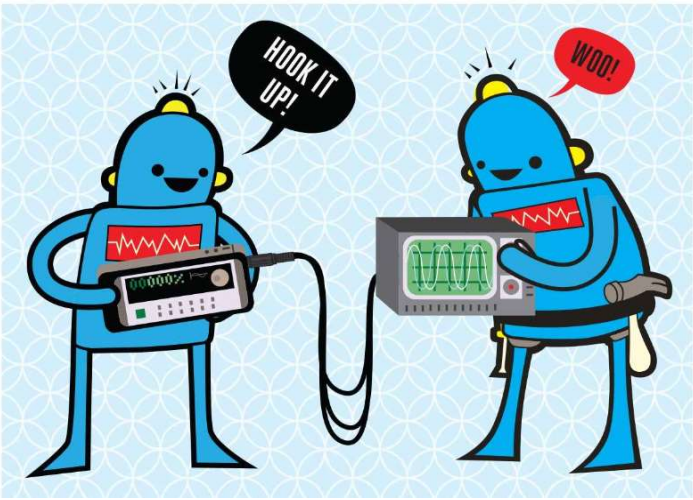
Step 4: Circuit Design

```
M1 3 2 0 0 nch W=1.2u L=0.6u AS=2.16p PS=4.8u AD=2.16p PD=4.8u
M2 3 2 1 1 pch W=1.8u L=0.6u AS=3.24p PS=5.4u AD=3.24p PD=5.4u
CL 3 0 0.2pF

VDD 1 0 3.3
VIN 2 0 DC 0 PULSE (0 3.3 0ns 100ps 100ps 2.4ns 5ns)

.LIB '../mod_06' typical

.OPTION NOMOD POST INGOLD=2 NUMDGT=6 BRIEF
.DC VIN 0V 3.3V 0.001V
.PRINT DC V(3)
.TRAN 0.001N 5N
.PRINT TRAN V(2) V(3)
.END
```

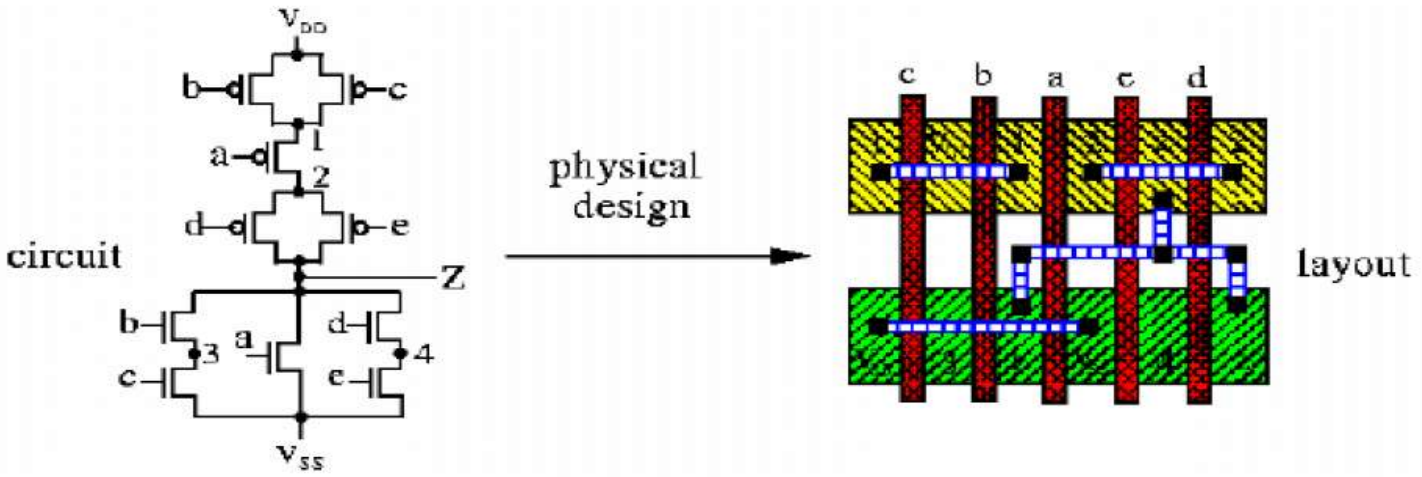






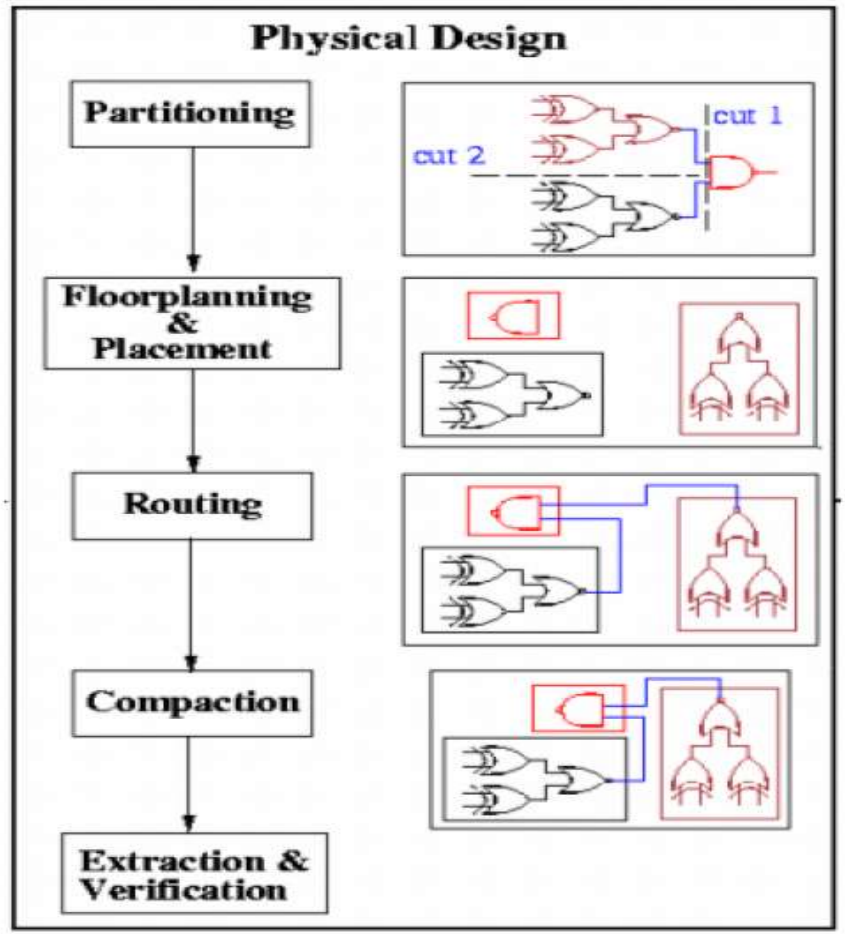


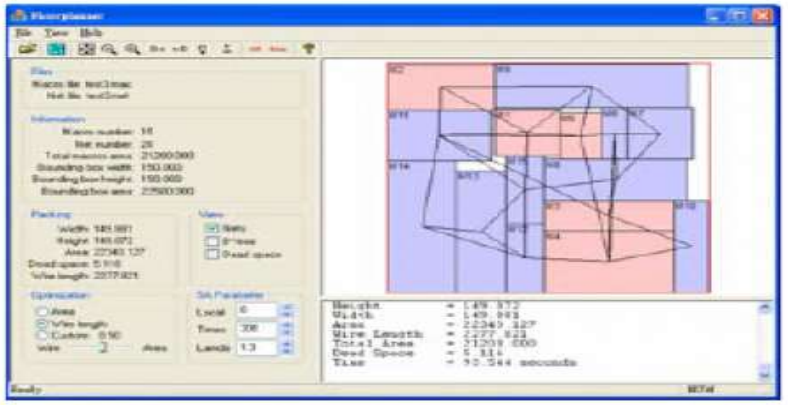
Step 5-1: Physical Design



- Physical design converts a circuit description into a geometric description.
- The description is used to manufacture a chip.
- Physical design cycle:
  1. Logic partitioning
  2. Floorplanning and placement
  3. Routing
  4. Compaction
- Others: circuit extraction, timing verification and design rule checking

Example: Physical Design (Place & Route)



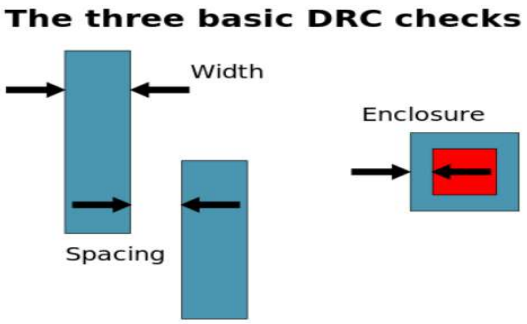


B*-tree based floorplanning system

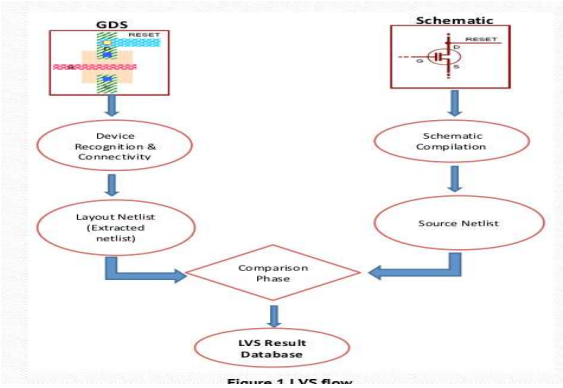
A routing system

Step 5-2: Physical Verification and Signoff

- DRC



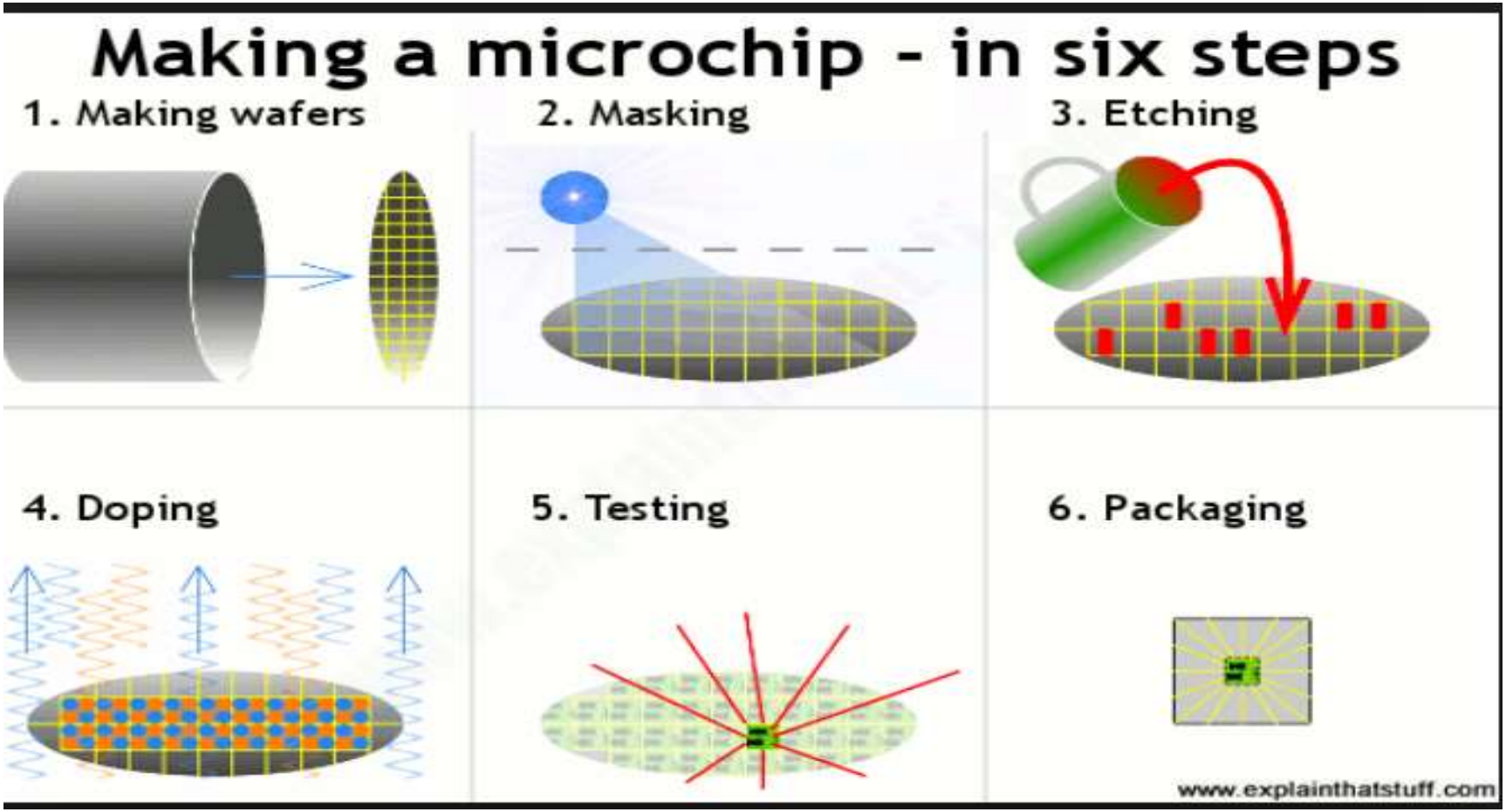
- LVS



- ERC

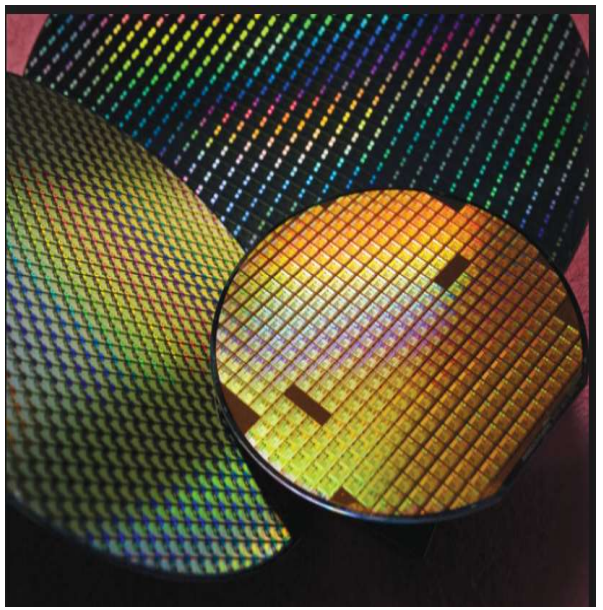
- Chip Finishing and Signoff
- Tapeout to foundry

VLSI Manufacturing (Coming Step 6 and 7)



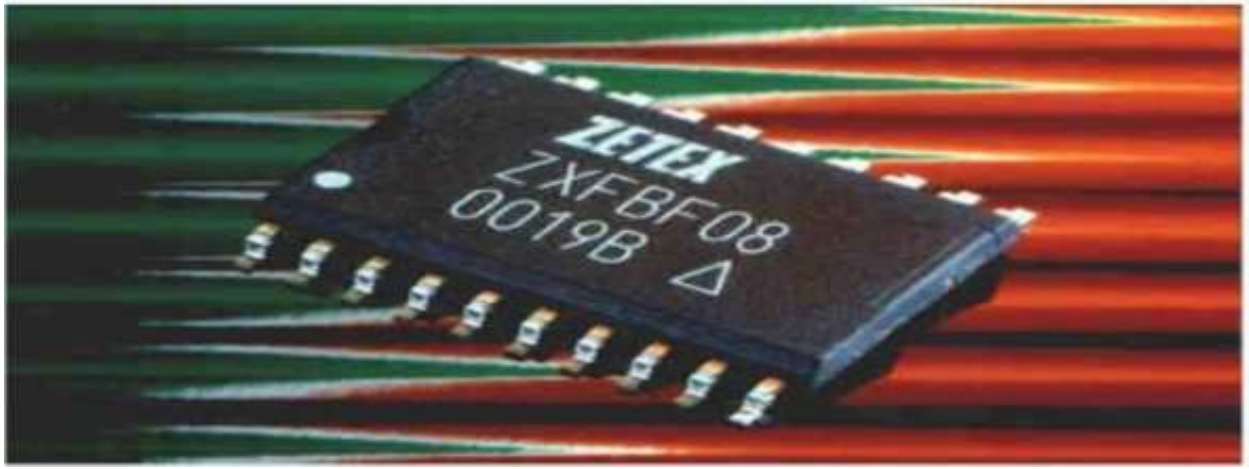
Step 6: Fabrication

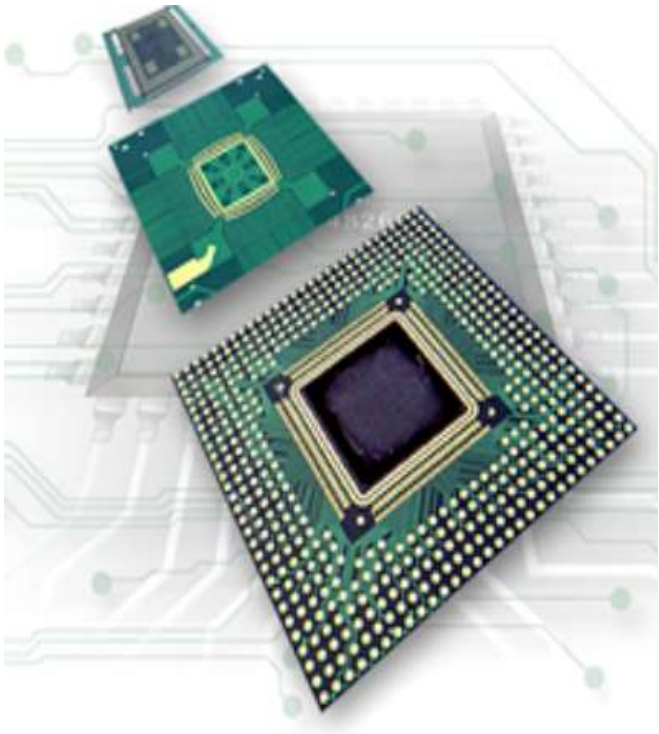
- After layout and verification, the design is ready for fabrication (called tapeout).
- Layout data is converted into photo-lithographic masks.



Step 7: Packaging and Testing

- After fabrication, each die is tested.
- The wafer is diced into individual chips.
- Each chip is packaged and tested.

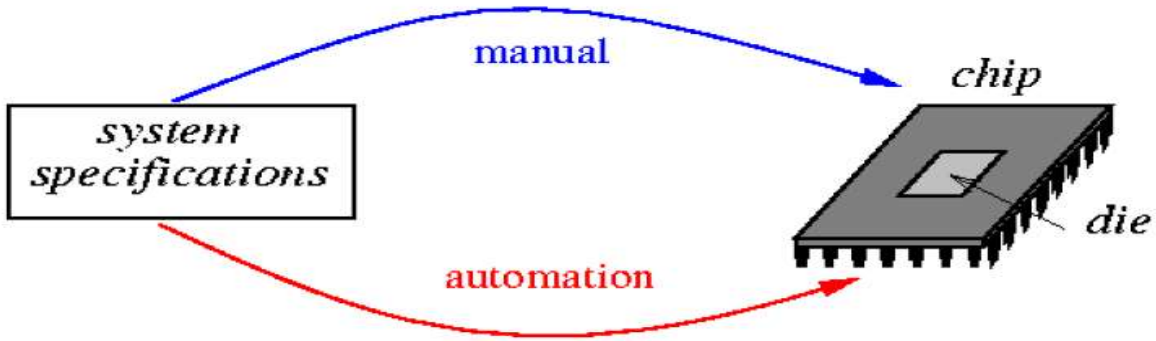




Intel: The Making of a Chip with 22nm/3D (Video)

- https://www.youtube.com/watch?v=d9SWNLZvA8g

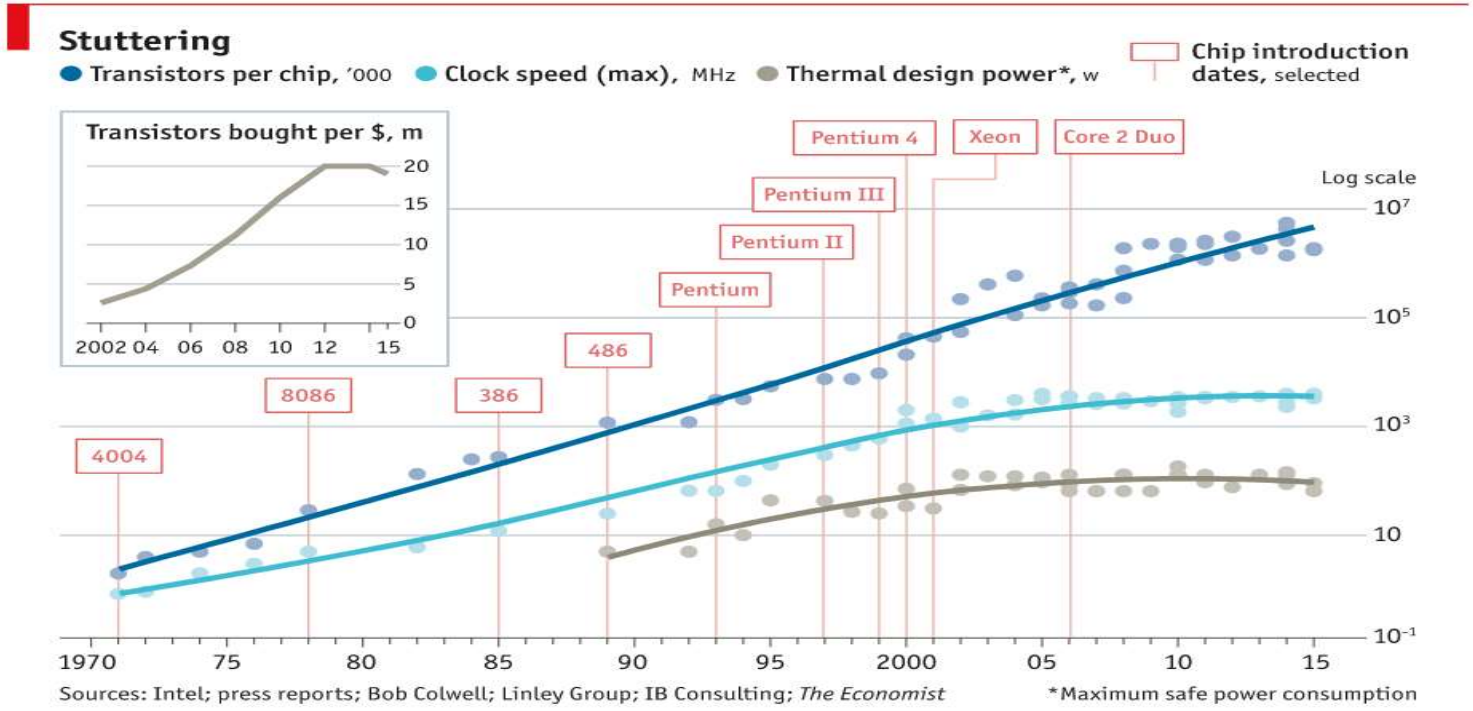
EDA Challenges and Future Trend



- Several conflicting considerations:
  - **Design complexity:** large number of devices/transistors
  - **Performance:** optimization requirements for high performance
  - **Time-to-market:** about a 15% gain for early birds
  - **Cost:** die **area**, packaging, testing, etc.
  - Others: power, signal integrity (noise, etc), testability, reliability, manufacturability, etc.

Moore's Law: Driving Technology Advances

- Logic capacity doubles per IC at a regular interval
  - Moore: Logic capacity doubles per IC every two years (1975)
  - D. House: Computer performance doubles every 18 months (1975)



Technology Roadmap for Semiconductors

Year	1997	1999	2002	2005	2008	2011	2014
Technology node (nm)	250	180	130	100	70	50	35
On-chip local clock (GHz)	0.75	1.25	2.1	3.5	6.0	10	16.9
Microprocessor chip size (mm^2)	300	340	430	520	620	750	901
Microprocessor transistors/chip	11M	21M	76M	200M	520M	1.40B	3.62B
Microprocessor cost/transistor ($\times 10^{-8}$ USD)	3000	1735	580	255	110	49	22
DRAM bits per chip	256M	1G	4G	16G	64G	256G	1T
Wiring level	6	6–7	7	7–8	8–9	9	10
Supply voltage (V)	1.8–2.5	1.5–1.8	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6	0.37–0.42
Power (W)	70	90	130	160	170	175	183

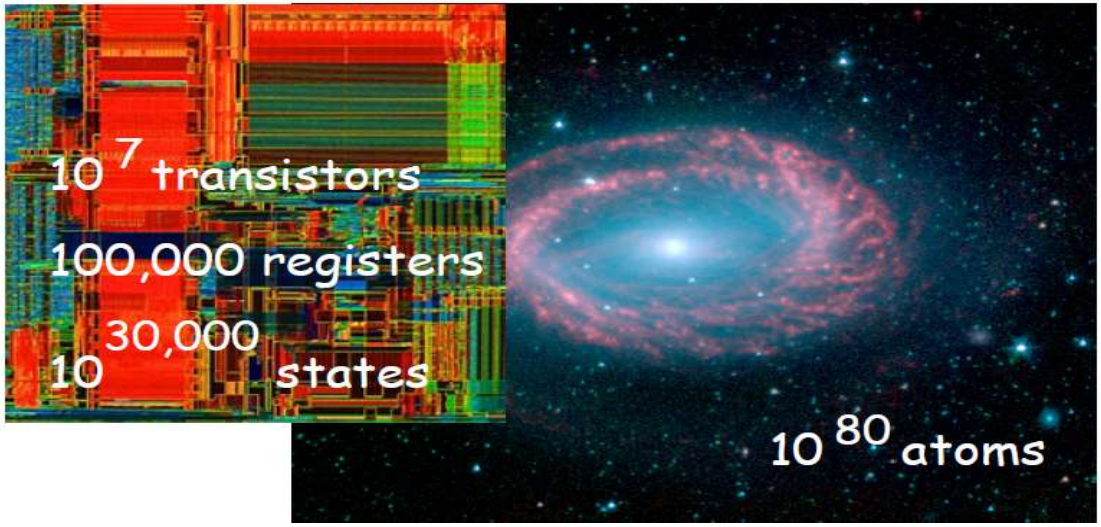
- Source: International Technology Roadmap for Semiconductors, Nov, 2002. http://www.itrs.net/ntrs/publntrs.nsf
- Deep submicron technology: node (**feature size**) < 0.25 μm
- Nanometer Technology: node < 0.1 μm

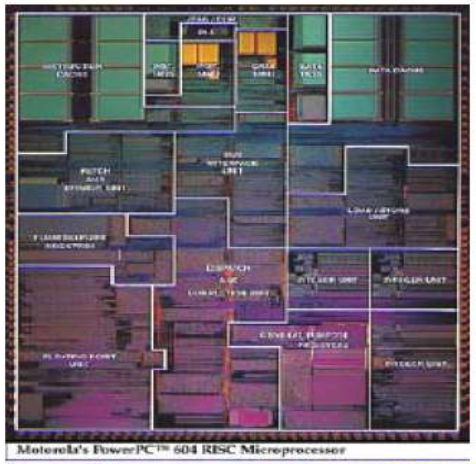
Nanometer Design Challenges

- In 2005, feature size ≈ 0.1 μm, μ P frequency ≈ 3.5 GHz, die size ≈ 520 mm^2, μ P transistor count per chip ≈ 200M, wiring level ≈ 8 layers, supply voltage ≈ 1 V, power consumption ≈ 160 W.
  - **Chip complexity**
    - **effective design and verification methodology? more efficient optimization algorithms? time-to-market?**
  - **Power consumption**
    - **power & thermal issues?**
  - **Supply voltage**
    - **signal integrity (noise, IR drop, etc)?**
  - **Feature size, dimension**
    - **sub-wavelength lithography (impacts of process variation)? noise? wire coupling? reliability? manufacturability? 3D layout?**
  - **Frequency**
    - **interconnect delay? electromagnetic field effects? timing closure?**

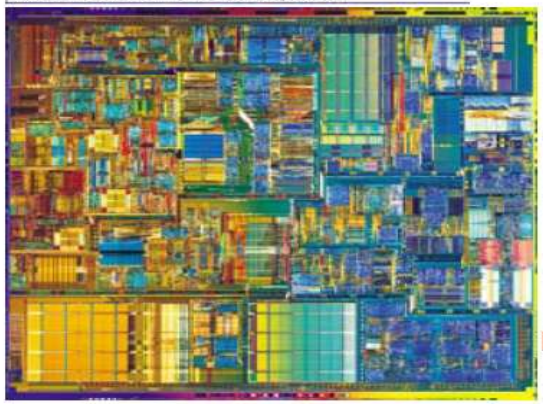
Design Complexity Challenges

- Design issues
  - Design space exploration
  - More efficient optimization algorithms
- Verification issues
  - State explosion problem
  - For modern designs, about 60%-80% of the overall design time was spent on verification; 3-to-1 head count ratio between verification engineers and logic designers





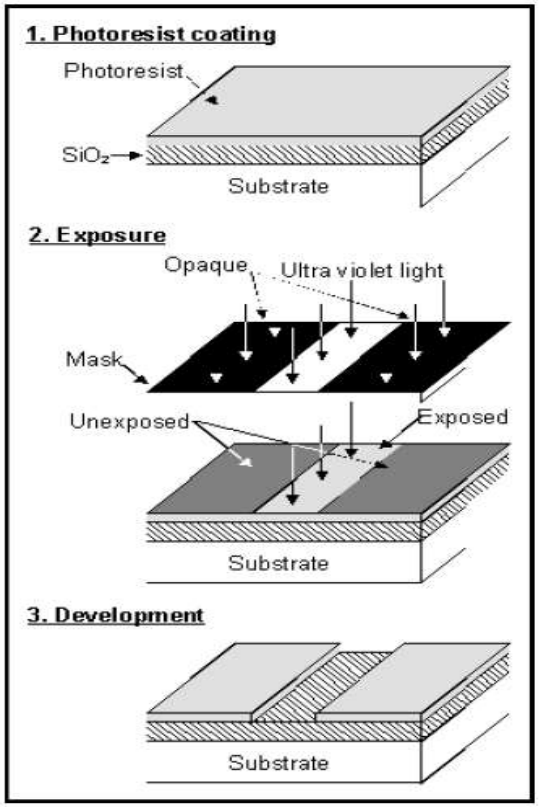
PowerPC 604

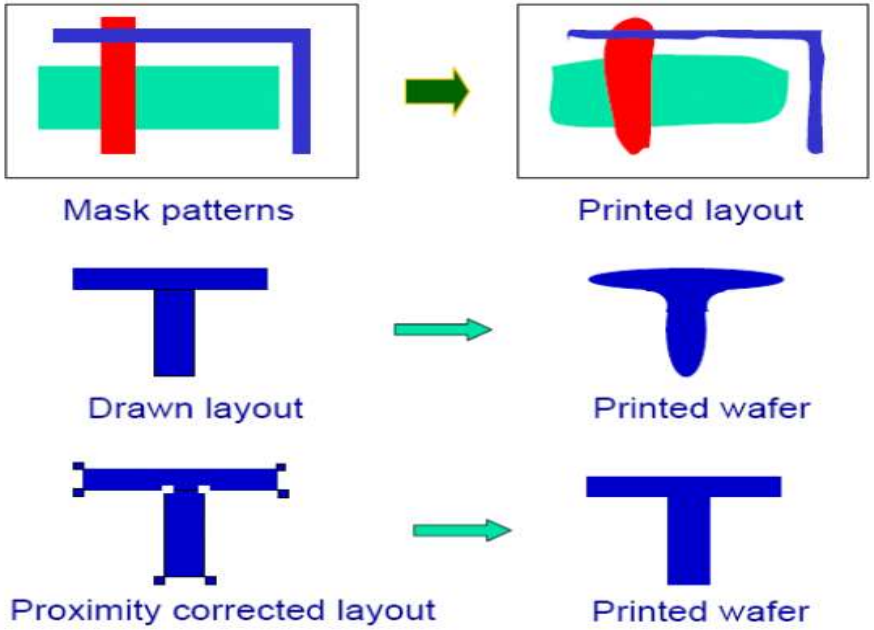


Pentium 4

Semiconductor Fabrication Challenges

- Feature-size shrinking approaches physical limitation

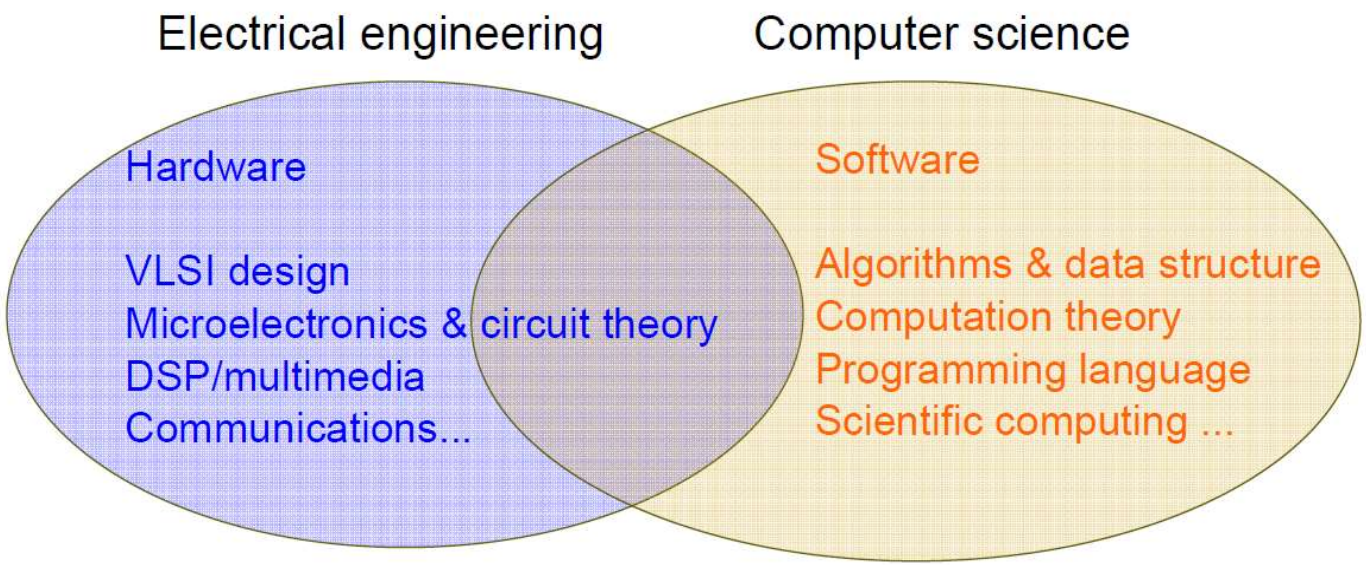




VLSI CAD Engineering

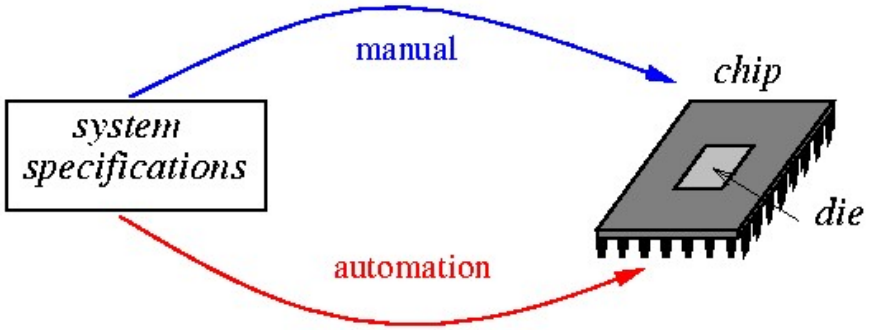
Introduction

- EDA, where HW and SW meet each other



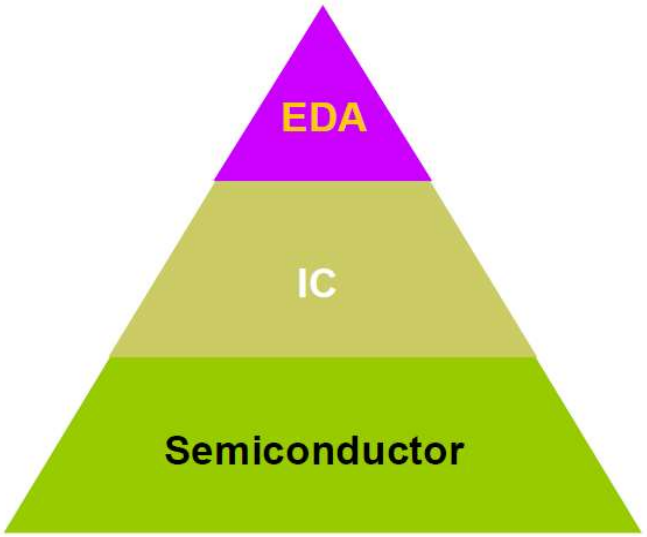
EDA in Chip Design

- EDA is concerned about HW/SW design in terms of
  - Correctness
  - Productivity
  - Optimality
  - Scalability



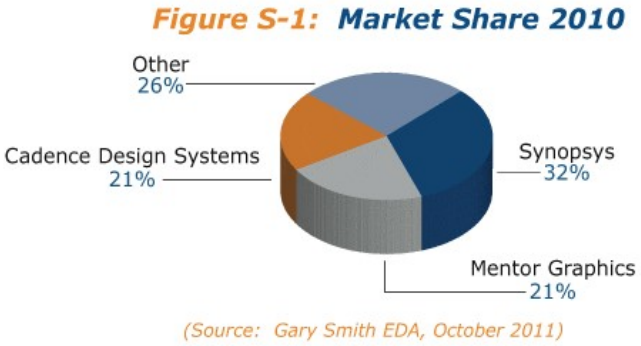
EDA and Industries

- EDA (in a strict sense) and industries
  - Impact - solving a problem may benefit vast electronic designs



EDA Vendors and Tools Development

- List of EDA Companies
- EDA's big three:
  - Cadence
  - Synopsys
  - Mentor

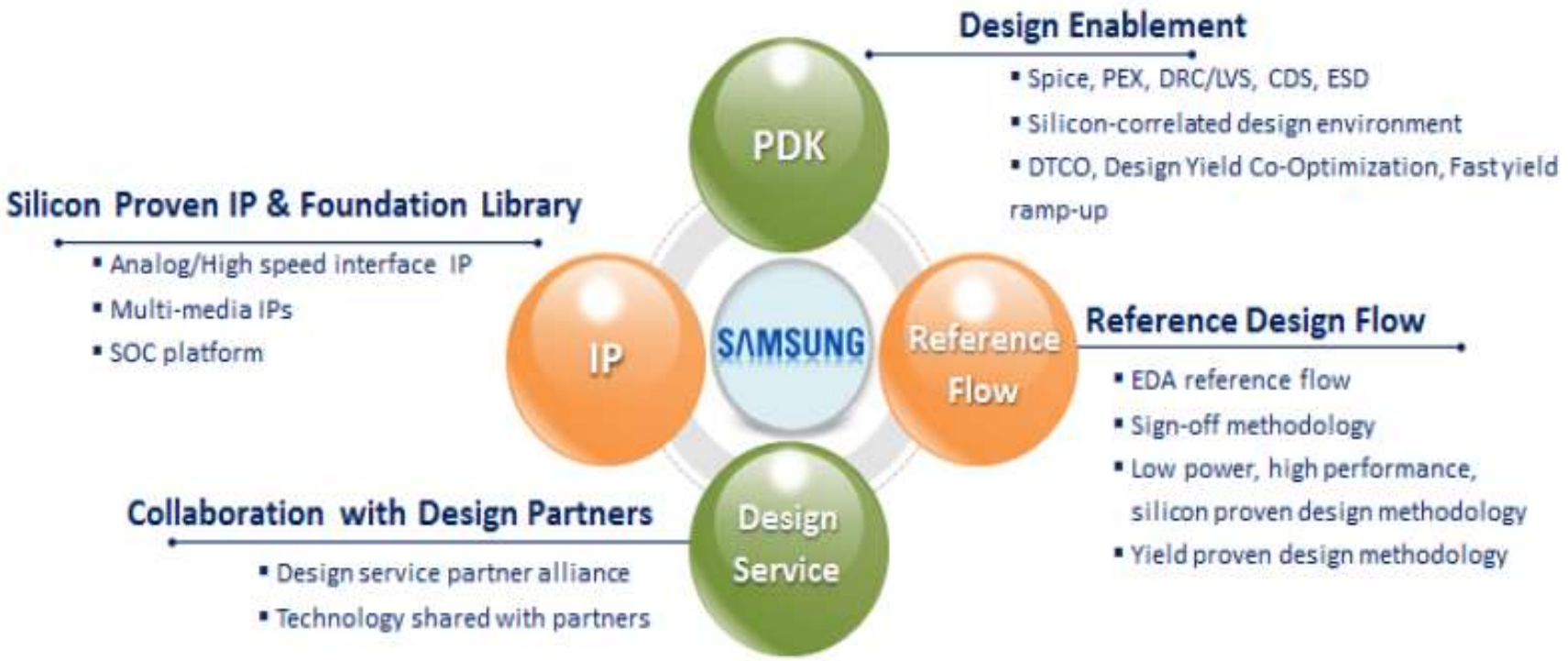


- EDA R&D
- Application Engineer

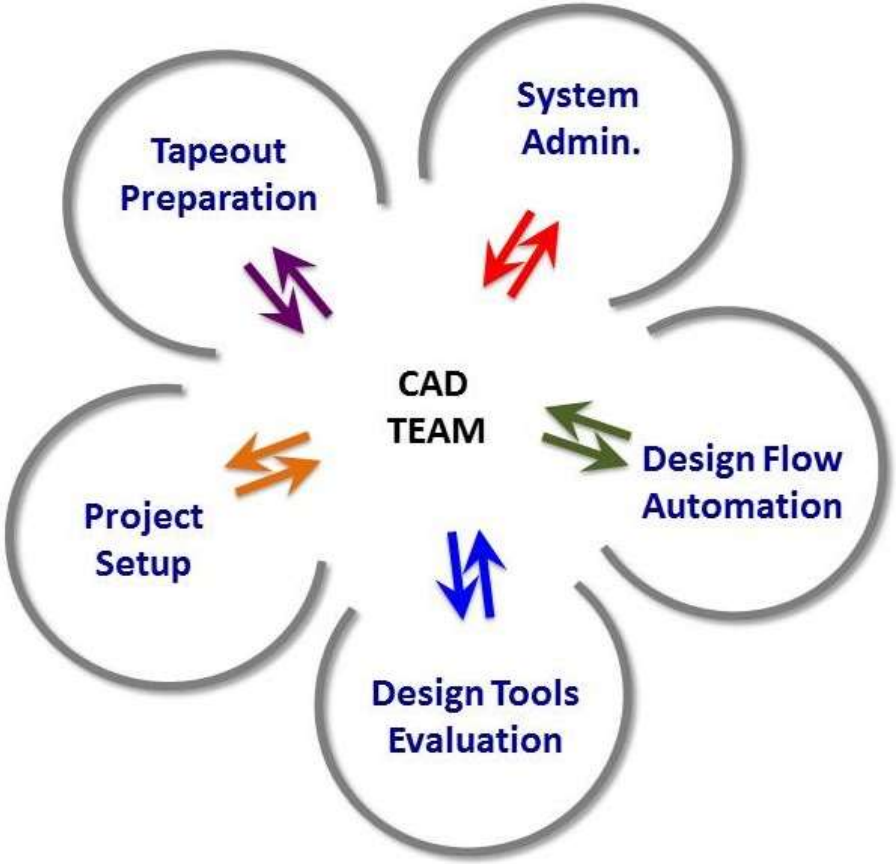
- Lots of Mergers and Acquisitions

Foundry PDK and IP Reuse

- Full spectrum of foundry design ecosystem



CAD Design Enablement



- Work with IT closely (license, network, disk space, remote site, revision control, security …)
- With deep understanding of chip design and EDA tool capabilities make sure to set up and automate all flows running smoothly till successfully tapeout to foundry
- Interfaces between the design teams and EDA vendors to evaluate the design tools that ensure the correct tools are set up for the design project.
- Must be good at:
  - Strong system admin (plus)
  - Solid understanding the chip design methodology and implementation
  - Excellent on programming and scripting
  - Good communication Skill

CAD as Career

- This career field would appeal to someone who enjoys problem solving, both software and hardware and working with engineers
- Someone has creative mindset, interested in exploring problem around them and solve it
- Someone interested in new technology at all levels and wants to learn new things everyday
- Someone has great satisfaction if they create something useful, or helped someone through automation
- Someone acts as “unsung hero in a successful tapeout”

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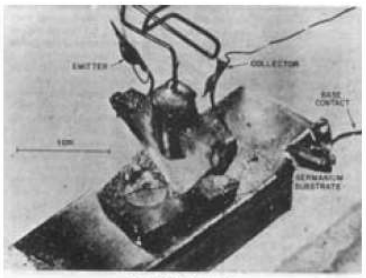
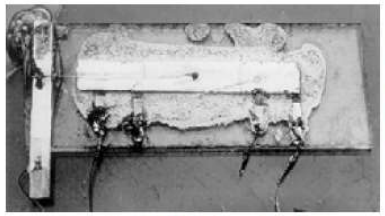
Appendix: Milestones of IC Industry

- **1947:** Bardeen, Brattain & Shockly invented the transistor, foundation of the IC industry.
- **1952:** SONY introduced the first transistor-based radio.
- **1958:** Kilby invented integrated circuits (ICs).
- **1965:** Moore's law.
- **1968:** Noyce and Moore founded Intel.
- **1970:** Intel introduced 1 K DRAM.

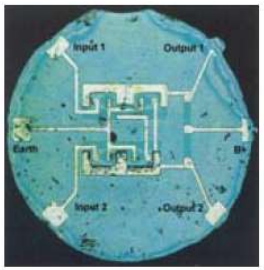
In 1956 John Bardeen, William Shockley and Walter Brattain shared the Nobel Prize in Physics for their discovery of the transistor.



First transistor



First IC by Kilby



First IC by Noyce

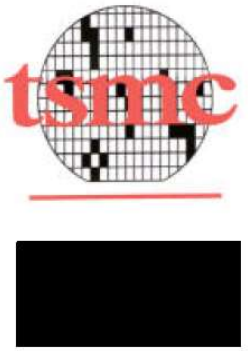
Appendix: Milestones of IC Industry (cont'd)

- **1971:** Intel announced 4-bit 4004 microprocessors (2250 transistors).
- **1976/81:** Apple II/IBM PC.
- **1985:** Intel began focusing on microprocessor products.
- **1987:** TSMC was founded (fabless IC design).
- **1991:** ARM introduced its first embeddable RISC IP core (chipless IC design).

Intel founders

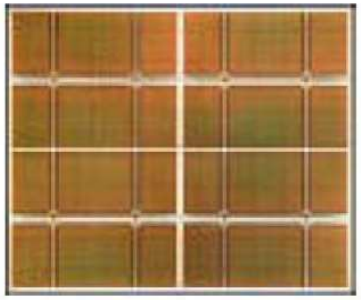
4004

IBM PC

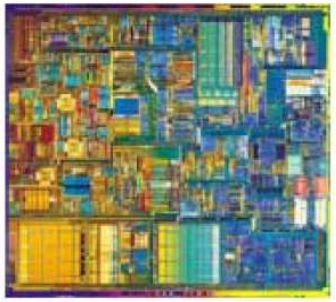


Appendix: Milestones of IC Industry (cont'd)

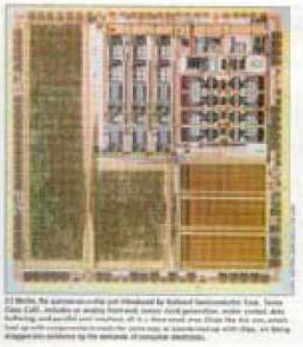
- **1996:** Samsung introduced 1G DRAM.
- **1998:** IBM announces 1GHz experimental microprocessor.
- **1999/earlier: System-on-Chip (SoC)** methodology applications.
- **2002/earlier: System-in-Package (SiP)** technology
- An Intel P4 processor contains 42 million transistors (1 billion by 2005)
- Today, we produce > 1 billion transistors per person.



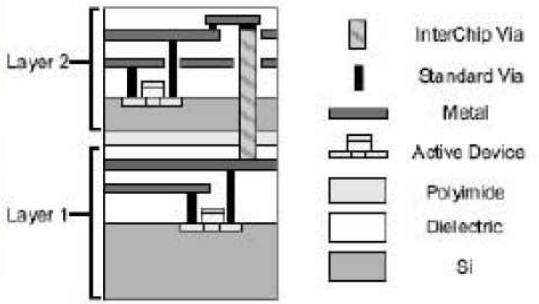
4GB DRAM (2001)



Pentium 4



Scanner-on-chip



System in Package (SiP)

Q&A